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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/750,320	12/31/2003	Edward A. Burton	884.C02US1	4675
21186	7590	06/16/2006	EXAMINER	
SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH, P.A. P.O. BOX 2938 MINNEAPOLIS, MN 55402			TRA, ANH QUAN	
			ART UNIT	PAPER NUMBER
			2816	

DATE MAILED: 06/16/2006

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**BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES**

Application Number: 10/750,320
Filing Date: December 31, 2003
Appellant(s): BURTON ET AL.

Robert Madden
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 04/07/06 appealing from the Office action mailed 09/22/05.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

6166577	Mizuno et al.	12-2000
6489833	Miyazaki et al.	12-2002
6333571	Teraoka et al.	12-2001

6337601	Klemmer	01-2002
6883078	Chen	04-2005
6708289	Kudo	03-2004

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1, 2, 6-18, 26, 27 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Mizuno et al. (USP 6166577).

As to claim 1, Mizuno et al. discloses in figure 12 an apparatus comprising: a substrate (circuit figure 12 is an integrated circuit, it is inherent that the circuit comprises substrate); a target timing circuit (OSC10) formed on the substrate, the target timing circuit having a frequency related to a target frequency; a leakage timing circuit (OSC20) formed on the substrate, the leakage timing circuit having a frequency related to a leakage current (the leakage current of the transistor is determined by voltage that is biased to it substrate or well. Therefore, the frequency of OSC circuit is also dependent on the leakage current of the transistor. See figure 4); and a control unit (CNT10, CNT20) to maintain a substantially constant ratio between the frequency related to the target frequency and the frequency related to the leakage current (*the*

ratios between the respective frequencies of the OSC10 and OSC20 and the frequency of CLK10 are constant. Therefore, the ratio between OSC10 and OSC20 is constant).

As to claim 2, figure 12 shows that the substrate comprises a semiconductor.

As to claim 6, figure 12 shows a self-timed circuit (LOG10) formed on the substrate, the self-timed circuit to operate at a frequency proportional to the target frequency.

As to claim 7, figures and 12 show that the control unit to provide a control signal to the substrate.

As to claim 8, figures 4 and 12 show that the substrate includes a plurality of coupled wells containing transistors (NMOS) of a matching type from the self-timed circuit, the target timing circuit, and the leakage timing circuit.

As to claim 9, figures 4 and 12 show that the transistors are all of the matching type.

As to claim 10, figures 4 and 12 show a well control unit (the BGEN circuit in CNT10 and CNT20) to provide a bias to the plurality of coupled wells.

As to claim 11, figure 4 shows the well comprises a p-type well.

Claim 12 recites similar limitations of claims 1 and 6. Therefore, it is rejected for the same reasons.

As to claims 13-15, the circuit figure 12 is used in microcomputer (see title). Therefore, the circuit is used in memory device. It is well known that communication device, i.e. cell phone comprises microcomputer. It is seen as an intended use of using circuit LOG10 in a memory, peripheral, or network communication interface.

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As to claims 16-18, figure 12 shows that the control unit (CNT10, CNT20) receives signal (S10) having the frequency related to the target circuit frequency and signal (S20) having frequency related to the leakage current.

Claim 26 recites similar limitations of claim 1. Therefore, it is rejected for the same reasons.

As to claim 27, figure 12 shows a processor (OSC30) formed on the substrate and having an operating frequency and a supply voltage (voltage supply to the substrate of transistors in the OSC30), changing the supply voltage to maintain a relationship between the target circuit frequency and the operating frequency.

As to claim 29, figures 4 and 14 shows the step of processing the target circuit frequency and a target ring oscillator frequency to generate a potential control signal to adjust a potential applied to a target ring oscillator, a leakage ring oscillator, and a target circuit that operates at the target circuit frequency.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (USP 6166577) in view of Klemmer (USP 6337601).

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As to claims 3 and 19, Mizuno et al.'s figure 4 shows that the target timing circuit comprises a ring oscillator. Figure 4 fails to shows that a counter is coupled to the ring oscillator. However, Klemmer's figure 3 shows a timing circuit having counter 82 coupled to the ring oscillator 80 for the purpose of increasing output frequency. Therefore, it would have been obvious to one having ordinary skill in the art to add a counter coupled between the oscillator OSC10 and CNT10 for the purpose of increasing the output frequency of the oscillator OSC10.

As to claim 4, Mizuno et al.'s figures 4 and 12 show that the leakage timing circuit (OSC20) comprises a ring oscillator.

As to claim 5, Mizuno et al.'s figure 12 shows that the frequency related to the leakage current is substantially proportional to the leakage current.

As to claim 20, Mizuno et al.'s figure 4 shows that the leakage ring oscillator comprises delay line.

5. Claims 28 and 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mizuno et al. (USP 6166577).

Figure 12 fails to shows a communication circuit formed on the substrate. However, it is well known in the art that communication circuit, i.e. cell phone comprises microcomputer. Mizuno et al.'s figure 12 has the advantage of reduce power consumption. Therefore, it would have been obvious to one having ordinary skill in the art to use Mizuno et al.'s microcomputer that comprises circuit figure 12 in a communication circuit for the purpose of reducing power consumption.

(10) Response to Argument

Appellants argue on page 12 that the cited references fail to teach “a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current”. The Examiner respectfully disagrees. Mizuno et al.’s figure 12 shows circuit OSC20 (leakage timing circuit), which has a similar structure as circuit OSC1 shown in figure 4, formed on the substrate. Since OSC20 is an integrated circuit, it is inherent that OSC20 is formed on substrate. Voltages BP20 and BN20, which are biased to backgates of transistors in OSC20, control the frequency of circuit OSC20. Mizuno et al. teaches in column 8, lines 50-55, that the level of the backgate bias voltage will control the threshold of the transistors. Furthermore, Teraoka et al.’s figures 3A-3C also teaches that the level of the backgate bias voltage controls the threshold of the transistors, and Miyazaki et al.’s figure 20 shows the relationship between the threshold of transistor and its leakage current. Thus, Teraoka et al. and Miyazaki et al. teach that the backgate bias voltage controls the leakage current of transistor. As stated above, Mizuno et al. discloses that the backgate bias voltage also control the frequency of transistor. Thus, the frequency of the transistor corresponds to its leakage current because they are both related to the backgate bias voltage. Therefore, the prior art above teaches that frequency of OSC20 is related to the leakage currents of transistors in OSC20.

Similar response is applied to Appellant’s arguments on pages 14-15 stating that the combination of Mizuno et al and Klemmer fails to teach “a leakage timing circuit formed on the substrate, the leakage timing circuit having a frequency related to a leakage current”.

Appellants further argue that “the final office action fails to provide specific, objective, evidence of record for a finding of a description, suggestion, or motivation to combine Mizuno et

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al. the Klemmer”. The examiner respectfully disagrees. Mizuno et al.’s figure 12 shows clock generation circuit having phase locked loop structure. Klemmer’s figure 3 shows a phase locked loop having counter 82 coupled to the ring oscillator for increasing the frequency ratio between the input and output of the phase locked loop. One skilled in the art would have motivated to add a counter coupled to Mizuno et al.’s OSC10 or OSC20 in order to increasing frequency ratio between signal CLK10 and output of OSC10 or OSC20.

Appellants argue that the combination of Mizuno et al. the Klemmer references would destroy the stated purpose in Mizuno et al. of locking the frequency of OSC1 oscillator to the frequency of output CLK1. The Examiner respectfully disagrees. One skilled in the art would have added the counter to the output of Mizuno et al.’s OSC1 if the frequency of CLK1 is lower than its desired frequency in order to maintain the desired frequency at the output of OSC1, or if a higher output frequency at OSC1 is needed. In either case, the modified circuit of Mizuno et al. would clearly be operated.

Appellants challenge the official notice taken that Mizuno et al.’s circuit can be use in communication circuit. Kudo taught in col. 15, lines 32-37, that microcomputer can be used in cell phone, and Chen teaches in column 1, lines 14-16, that microcomputer can be used in cell phone, communication circuit. The communication limitations are merely seen as a statement of intended use. Clearly, as shown by the prior art, Mizuno et al.’s microcomputer, which comprises the circuit of figure 12, may be used in a communication circuit in order to reduce power consumption of that communication circuit. Thus, circuit such as LOG10 is considered as “communication circuit”.

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(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

(12) Conclusion

Mizuno et al. and the modified Mizuno et al. teach all limitations of the claims.

Therefore, it is believed that the rejections should be sustained.

Respectfully submitted,



QUAN TRA
PRIMARY EXAMINER
Art Unit 2816

Conferees:

Tim Callahan



Mack Ricky



Quan Tra

